AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for bridging the dead-band when a signal having a first frequency is compared against a signal having a second frequency, said method comprising:

developing from said second frequency signal a pair of phase related signals each of said phase related signals having the same frequency but phase shifted from each other, said same frequency being controlled by said second frequency signal; [[and]]

comparing said first signal against each of said phase related signals to generate [[an error signal which]] a quadrature vector that rotates when said first and second frequency signals differ in frequency from each other; and

resolving a metastability by allowing a portion of a rotation of the quadrature vector before asserting an output signal.

2. (Original) The method of claim 1 wherein said method further comprises:

generating a control signal when said quadrature rotation is outside a certain limit.

3. (Original) The method of claim 2 wherein said certain limit is controllable.

4. (Original) The method of claim 2 wherein said certain limit is different for different quadrature rotation directions.

5. (Currently Amended) The method of claim 2 wherein said comparing comprises:

generating the output signal[[s]] based on a mismatch[[es]] between said first frequency signal and each of said generated phase-shifted signals;

deriving a frequency divided signal from said first frequency signal; and

clocking said output signal[[s]] against said frequency divided signal.

6. (Original) The method of claim 5 further comprising:

adjusting said frequency divided signal to control said certain limit.

7. (Currently Amended) A system for bridging the dead-band when a first signal having a first frequency is compared against a second signal having a second frequency, said system comprising:

circuitry for developing from one of said signals a pair of phase related signals each said phase related signal having the same frequency as said signal from which said phase related signals and developed; [[and]]

comparing circuitry for comparing the other of said signals against each of said phase related signals to generate [[an error signal which]] a quadrature vector that rotates when said first and second signals differ in frequency from each other; and

circuitry for allowing a portion of a rotation of the quadrature vector before asserting an output signal to resolve a metastability.

8. (Original) The system of claim 7 further comprising:

generating circuitry for generating a control signal when said quadrature rotation is outside a certain limit.

9. (Original) The system of claim 8 wherein said certain limit is controllable.

10. (Original) The system of claim 8 wherein said certain limit is different for different quadrature rotation directions.

11. (Currently Amended) The system of claim 8 wherein said comparing circuitry comprises:

circuitry for generating the output signal[[s]] based on a mismatch[[es]] between said other of said signals and each of said generated phase-shifted signals;

circuitry for deriving a frequency divided signal from said other of said signals; and

circuitry for clocking said output signal[[s]] against said frequency divided signal.

12. (Original) The system of claim 11 further comprising:

circuitry for adjusting said frequency divided signal to control said certain limit.

13. (Currently Amended) A circuit for comparing two asynchronous signals, said circuit comprising:

a phase detector;

a frequency detector for detecting both the magnitude and polarity of any frequency difference between said signals, said frequency detector yielding control of said circuit to said phase detector when the frequency difference is within a dead-band region; and

circuitry for [[bridging]] delaying a glitch[[es]] within said dead-band for a period of time to [[insure that said frequency difference is not outside a certain limit]] allow the glitch to resolve.

14. (Currently Amended) The circuit of claim 13 [[wherein said bridging circuitry]] further comprising: [[comprises:]]

circuitry for developing from a first one of said signals a pair of phase related signals each said phase related signal having the same frequency as first one of said signals but phase shifted 90 degrees therefrom; and

circuitry for comparing a second one of said signals against each of said phase-related signals to generate a quadrature rotating error signal when said compared signals differ in frequency from each other[[, wherein the speed of said quadrature rotation controls said certain limit]].

15. (Canceled)

16. (Canceled)

17. (Original) The circuit of claim 14 wherein said comparing circuitry comprises:

circuitry for generating output signals based on mismatches between a second one of said signals and each of said generated phase-shifted signals;

circuitry for deriving a frequency divided signal from said first one of said signals; and

circuitry for clocking said output signals against said frequency divided signal.

18. (Original) The circuit of claim 15 further comprising:

circuitry for adjusting said frequency divided signal to control said certain limit.

19. (Currently Amended) A method for comparing two asynchronous signals, said method comprising the steps of:

comparing the phase of said signals;

comparing both the magnitude and polarity of any frequency difference between said signals to yield control to said phase comparison when the frequency difference is within a dead-band region;

generating quadrature signals from one of said compared signals;

comparing the other of said signals against said quadrature signals to yield a signal which has a speed of rotation having a relationship to any mismatch between said signals, and

[[bridging]] delaying a glitch[[es]] within said dead-band for a period of time to [[insure that said compared signals are not outside a certain limit,]] allow the glitch to resolve, said [[bridging]] delaying a function of said speed of said phase rotation.

20. (Canceled)

21. (Currently Amended) A VCO circuit having a VCO output voltage and a reference voltage, said circuit comprising:

a phase detector;

a frequency detector for detecting both the magnitude and ~~ploarity~~ polarity of any frequency difference between said reference signal and said VCO output voltage, said frequency detector yielding control of said circuit to said phase detector when the frequency difference is within a dead-band region; and

circuitry for [[bridging]] delaying a glitch[[es]] within said dead-band for a period of time to [[insure that said frequency difference is not outside a certain limit]] allow the glitch to resolve.

22. (Currently Amended) The VCO circuit of claim 21 [[wherein said bridging circuitry comprises:]] further comprising:

circuitry for developing from said VCO output voltage a pair of phase related signals each said phase related signal having the same frequency as said VCO output voltage but phase shifted 90 degrees therefrom; and

circuitry for comparing said reference signal against each of said developed signals to generate a quadrature rotating an error signal when said reference signal and said VCO output voltage are out of frequency with each other[[, wherein the speed of said quadrature rotation controls said certain limit]].